S E R V I C E N O T E

SUPERSEDES: None

8665A Synthesized Signal Generator

Jitter Is Normal For Internal Modulation Source

Duplicate Service Notes:
8643A-02
8644A-02
8644B-02
8645A-03
8664A-02
8665B-02
70320A-02
70322A-02

Parts Required: None

Situation:
The internal modulation source (also known as the NSM Oscillator, Modulation Distribution Module or STD MOD/NSM OSC) in this instrument utilizes digital waveform synthesis to develop sine, square, ramp, triangle, and noise waveforms at rates up to 400 kHz. Sinewaves and noise produced by this technique have excellent time stability (no jitter). Square, ramp, and triangle waveforms have a certain amount of jitter. It is normal for this jitter to occur utilizing this type of synthesis.

Continued

DATE: 31 March 1993

ADMINISTRATIVE INFORMATION

SERVICE NOTE CLASSIFICATION:

INFORMATION ONLY

AUTHOR:	ENTITY:	ADDITIONAL INFORMATION:
LHL	1000	

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Jitter occurs when the frequency of these waveforms is not harmonically related to the DAC clock frequency (which is exactly [2^24]/10 or 1,677,721.6 Hz). The value of this jitter will be one clock cycle of the DAC (1/1.677 MHz or approximately 600 nanoseconds) for square and triangle waveforms. This value doubles to approximately 1200 nanoseconds when using ramp waveforms due to the fact that there is only one fast transition per cycle of this non-symmetrical waveform. The sinewave have no instantaneous transitions and therefore has no jitter.

For example, if we choose a frequency of 24.5 kHz, this frequency divided into the clock yields a non-integer relationship (68.4784). Therefore the fast edges of the square or ramp waveforms, and peaks of the triangle wave, do not always align with the clock. The result is that an occasional fast transition occurs one DAC cycle before or after the correct time.

The jitter produced by digital waveform synthesis does not occur on every cycle. The severity of the jitter is predictable by calculating how far from a perfect frequency relationship a particular waveform is from the clock frequency. If we choose a different frequency, such as 23.3 KHz, the jitter will almost be zero because the frequency relationship is nearly integral (72.0052). Since this frequency is harmonically related to the clock frequency the fast edges almost always coincide with the output clock of the DAC.

Solution/Action:
None